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Shifting Scan Quality Left: A Hierarchical RTL-Based Verification Framework with Proven Silicon Correlation

Sashaank Kasturirangan
Independent Researcher, USA

ABSTRACT: The relentless pursuit of higher integration densities in the semiconductor industry, marked by the transition to sub-5nm process nodes, has pushed traditional Design for Testability (DFT) methodologies to their breaking point. As System-on-Chip (SoC) designs scale to encompass billions of transistors and hundreds of heterogeneous Intellectual Property (IP) blocks, the conventional gate-level DFT insertion and verification flow has become a primary source of schedule unpredictability and late-stage design closure failures. This report presents a comprehensive analysis of the "Shift-Left" paradigm as applied to DFT, proposing a hierarchical, Register-Transfer Level (RTL)-based verification framework. By moving DFT architectural decisions, insertion, and design-rule checking (DRC) to the RTL stage, designers can concurrently optimize for power, performance, and area (PPA) while drastically reducing the time required for Automatic Test Pattern Generation (ATPG) and physical synthesis. The research explores the mechanisms of hierarchical partitioning, core-wrapping via IEEE 1500 standards, and the integration of functional fault grading to bridge the coverage gaps inherent in structural testing. Central to this framework is the concept of silicon correlation ensuring that pre-silicon RTL-based metrics accurately reflect post-silicon yield and diagnostic results. Through an examination of industrial case studies and recent advancements in Electronic Design Automation (EDA), this report demonstrates that a hierarchical RTL-based approach provides a scalable and predictable path to achieving zero-defect quality in modern high-performance computing and automotive applications.

KEYWORDS: Shift-Left DFT, Hierarchical Verification, RTL Scan Insertion, Silicon Correlation, Core Wrapping, ATPG Retargeting, Fault Grading, Silicon Lifecycle Management.

1. Introduction

The semiconductor design landscape is currently defined by the intersection of extreme complexity and compressed time-to-market requirements. As modern System-on-Chip (SoC) architectures evolve to support artificial intelligence (AI), high-performance computing (HPC), and autonomous driving, the density of transistors has reached a scale where monolithic design and test strategies are no longer viable. In this context, Design for Testability (DFT) has transitioned from a backend manufacturing requirement to a foundational architectural pillar. Historically, DFT was a sequential task, performed only after the functional design was synthesized into a gate-level netlist. However, this late-stage approach often leads to surprises like testability violations, timing bottlenecks, and congestion issues that require costly return-to-RTL iterations.

The "Shift-Left" methodology, which originated in the software development industry to mitigate the escalating costs of late-stage bug discovery, has been rapidly adopted by the EDA industry. In the realm of DFT, Shifting-Left involves conducting testability analysis, scan insertion, and verification early in the design cycle, specifically at the Register-Transfer Level (RTL). This proactive strategy allows designers to identify and resolve testability-resistant logic, optimize scan chain routing before physical placement, and validate test protocols using fast RTL simulations rather than slow, resource-intensive gate-level simulations (GLS).

A critical enabler of this Shift-Left movement is the adoption of hierarchical DFT. By partitioning a massive SoC into manageable, autonomous physical cores, the hierarchical approach enables parallel development and "DFT-complete" block delivery. Each core can be

individually wrapped, compressed, and verified, with the resulting patterns retargeted to the top-level pins during SoC integration. This "divide-and-conquer" methodology not only addresses the memory bottlenecks of modern ATPG tools but also enhances the predictability of the final silicon quality.

However, the efficacy of an RTL-based framework is ultimately determined by its silicon correlation. Correlation ensures that the fault coverage achieved in simulation translates into real-world defect detection on the manufacturing floor. This report delves into the structural requirements of this framework, focusing on the synergy between early RTL verification and the final post-silicon validation phase. By examining the roles of core-wrapping, advanced fault modeling, and functional fault grading, we outline a comprehensive strategy for shifting scan quality left while maintaining a proven link to silicon success.

2. The Economic and Technical Imperative of Shift-Left DFT

The transformation of the DFT flow is driven by both technical necessity and economic reality. In the semiconductor industry, the "Rule of Ten" suggests that the cost of detecting and fixing a defect increases tenfold at each subsequent stage of the product lifecycle from RTL to gate-level, from gate-level to silicon, and from silicon to the field.

Limitations of the Traditional Gate-Level Flow

Traditionally, DFT was performed after synthesis, as the gate-level netlist provided the necessary physical representation of the flip-flops and combinational logic. While this ensured that the scan chains were mapped to actual hardware, it introduced several critical risks. Discovery of Design Rule Check (DRC) violations such as uncontrolled clocks, un-resettable flip-flops, or combinational loops only after synthesis meant that designers had to modify the RTL and restart the synthesis process. In a design with hundreds of millions of gates, a single synthesis run can take days, making these iterations a significant schedule risk.

Furthermore, traditional gate-level ATPG suffers from a performance bottleneck. Monolithic ATPG requires the tool to load the entire flattened netlist into memory, which often exceeds the capacity of available hardware for modern multi-billion gate designs. This leads to longer runtimes, reduced tool responsiveness, and a lack of visibility into block-level testability issues until late in the cycle.

Theoretical Foundations of the Shift-Left Movement

The core principle of Shifting-Left in EDA is the concurrent execution of tasks that were once sequential. In the context of DFT, this means performing testability analysis while the functional RTL is still being authored. Early "Pre-DFT" DRC tools analyze the RTL for potential testability hurdles, ensuring that >99% of flip-flops in a block are scannable before they ever reach synthesis.

Metric	Traditional Gate-Level Flow	Shift-Left RTL Flow
DFT Insertion Stage	Post-Synthesis Netlist	Pre-Synthesis RTL
Verification Speed	Slow (Gate-Level Simulation)	Fast (RTL Simulation)
PPA Optimization	Localized (Post-Placement)	Holistic (Concurrent with Synthesis)
Error Discovery	Late (Costly Iterations)	Early (Proactive Resolution)

ATPG Capacity	Monolithic (Memory Bottlenecks)	Hierarchical (Distributed Memory)

The Shift-Left approach also allows for early PPA (Power, Performance, and Area) optimization. By inserting DFT logic at RTL, synthesis tools can account for the scan-path overhead during initial placement and routing, leading to a more optimal design closure. This is particularly vital in high-speed designs where the addition of a scan multiplexer in a critical path can lead to timing violations if not managed concurrently with functional logic optimization.

3. Hierarchical DFT Architecture and Core-Wrapping

To manage the complexity of modern SoCs, the design is typically partitioned into a hierarchy of physical blocks or cores. A hierarchical DFT framework leverages this structure to decentralize the test implementation process.

Partitioning and Core-Level Autonomy

Hierarchical DFT involves partitioning the design into autonomous, "DFT-complete" units. Each core is treated as an independent entity where scan chains are inserted, compression logic is added, and ATPG patterns are generated and validated. This allows for the parallelization of the DFT workload, as different teams can work on different cores simultaneously, improving overall design throughput.

One of the most significant advantages of this approach is the reduction in tool memory footprint. During top-level SoC integration, instead of loading the full gate-level netlist for every core, the tools use "gray-box" netlists or test models (e.g. tcd files). This enables the ATPG tool to focus only on the top-level interconnects and the necessary core-level interfaces, reducing memory requirements for a large SoC from over 100GB to less than 10GB.

Core-Wrapping Standards: IEEE 1500 and Beyond

To facilitate the isolation and testing of these individual cores, a standardized wrapping methodology is required. The IEEE 1500 standard provides a framework for core-level test wrappers, conceptually similar to the JTAG (IEEE 1149.1) boundary scan but optimized for internal SoC partitions.

The wrapper defines two primary modes of operation:

1. **INTEST (Internal Test):** In this mode, the core's internal logic is isolated from its external environment. Input wrapper cells drive the core's primary inputs with test stimulus, while output wrapper cells capture the core's responses. This is used for verifying the internal functionality and fault coverage of the core.

2. **EXTEST (External Test):** This mode focuses on the logic outside the cores, specifically the inter-core "glue logic" and routing. The internal scan chains of the cores are typically bypassed to reduce test time, while the wrappers are used to drive and capture data on the interconnects.

The structure of the wrapper cells can be either dedicated or shared. Shared wrapper cells reuse existing functional flip-flops near the core boundaries, which minimizes the area overhead and is ideal for area-constrained designs. However, dedicated wrapper cells, while adding a small amount of area, provide shorter wrapper chains and more predictable timing, which can be advantageous for high-speed critical signals.

Pattern Retargeting and Database Management

A cornerstone of the hierarchical framework is pattern retargeting. Patterns are generated at the core level and stored in a pattern database (PATDB) format. When the cores are integrated into the SoC, these patterns are retargeted or mapped to the top-level pins. This process allows for the reuse of the same pattern set for identical instances of a core (e.g. multiple identical processor cores in an 8-core CPU), ensuring that the total pattern count and thus the test time on the manufacturing floor does not scale linearly with the number of cores.

RTL-Based DFT Verification Framework

The efficacy of a Shift-Left strategy is predicated on a

robust verification framework that can analyze and validate test structures directly at the RTL stage.

Early Design-Rule Checking (DRC) and Scannability

RTL-based verification begins with "Pre-DFT" DRCs. These checks analyze the HDL code to identify structures that would impede testability after synthesis. Key focus areas include:

- **Clock and Reset Control:** Ensuring that all sequential elements can be reliably controlled during the scan shift and capture phases. If a flip-flop's clock is driven by internal combinational logic that cannot be bypassed in test mode, it becomes a "non-scan" flop, reducing coverage.
- **Combinational Loops and Latches:** Identifying asynchronous loops and latches that could cause non-deterministic behavior during ATPG simulation.
- **Connectivity Analysis:** Verifying that the test signals (e.g., Scan Enable, Test Mode) are properly propagated through the design hierarchy.

By achieving early DRC closure at RTL, designers can ensure that the final netlist will have high scannability (often exceeding 99.5%), significantly reducing the risk of coverage loss.

Hierarchical Error Diagnosis at RTL

Verification at RTL also extends to error diagnosis. Algorithms that target RTL descriptions exploit the inherent hierarchy of the design to locate functional or test-protocol errors. Research has shown that diagnosis at RTL is not only faster but often more accurate than gate-level diagnosis, as it operates at a higher level of abstraction and avoids the noise of synthesis optimizations. Techniques such as X-lists are used to capture the effects of design errors within specific components, allowing for rapid identification and remediation of bugs before they are propagated into the netlist.

Test Point Insertion (TPI) and SCOAP Metrics

To address "random-pattern-resistant" (RPR) faults, logic areas that are difficult to control or observe using standard pseudo-random patterns, test points are inserted into the design. In an RTL-based flow, Test Point Insertion (TPI) is performed on the original specification.

TPI tools utilize controllability and observability metrics (such as SCOAP Sandia Controllability/Observability Analysis Procedure) to identify the optimal locations for test points. By adding control points (to force a signal to a specific value) and observation points (to capture a signal's state), designers can achieve near-complete fault coverage with minimal area overhead. Experiments on industrial designs have shown that RTL-based TPI can improve DC coverage by as much as 2%, which is often the difference between meeting or missing a quality target.

4. Advanced Fault Modeling and Scan Compression

As process nodes shrink to 5nm and below, the types of defects that can occur during manufacturing become increasingly complex. A Shift-Left framework must support advanced fault models that go beyond the basic "stuck-at" model to ensure high silicon quality.

Multi-Model Fault Coverage

While the stuck-at fault model remains the industry standard, it is no longer sufficient to capture all physical defects in advanced nodes. Modern DFT frameworks incorporate a suite of models:

- **Transition Delay Faults:** These target timing errors where a signal is too slow to rise or fall within the required clock period. Testing these requires "at-speed" patterns using Launch-off-Capture (LOC) or Launch-off-Shift (LOS) methodologies.
- **Bridging Faults:** Shorts between adjacent signal lines, which are common in dense metal layers. These are detected by observing the logical interference between the affected nets.
- **Cell-Aware Faults:** These target defects *inside* the standard cells themselves, rather than just on the interconnects. As transistors become smaller, internal cell defects represent a larger percentage of total failures.
- **IDDQ Faults:** These detect abnormal leakage currents that indicate gate-oxide breakdowns or other parametric defects.

Scan Compression and Test Data Volume (TDV)

The volume of test data required for a billion-gate SoC is immense, often exceeding the memory capacity of Automatic Test Equipment (ATE). Scan compression is used to reduce both the test data volume and the test application time.

In a compressed scan architecture, a decompressor at the input expands a few tester channels into hundreds or thousands of short internal scan chains. A compactor at the output then reduces the responses into a small number of signatures for comparison. Hierarchical DFT environments often use distributed compression logic at the core level, which reduces routing congestion compared to centralized top-level compression. This approach has been shown to achieve compression ratios of 100x or more, making the testing of massive designs commercially viable.

5. Bridging the Gap: Functional Fault Grading and Silicon Correlation

A primary challenge in shifting scan quality left is ensuring that the early RTL metrics correlate with the final silicon results. Functional fault grading and hybrid verification strategies play a crucial role in this bridge.

Functional Fault Grading (FFG)

Structural ATPG patterns are designed to detect faults by controlling and observing internal nodes via scan chains. However, some areas of the design, such as analog/mixed-signal blocks or high-speed IO, may have limited scan observability. Functional fault grading involves using existing functional validation patterns (e.g., boot-up sequences, loopback tests) and determining their effectiveness at detecting manufacturing defects.

By injecting faults into the RTL and running functional simulations, designers can identify "incidentally detected" faults that ATPG might miss. This hybrid approach combining structural ATPG with functional patterns has been shown to increase overall fault coverage by nearly 1% and detect thousands of additional "DI" (det_implication) faults. More importantly, it allows the DFT and DV (Design Verification) teams to work in parallel, using the same RTL stimulus to accelerate the development cycle.

The Role of Gate-Level Simulation (GLS) in Correlation

While the goal of Shift-Left is to minimize the reliance on GLS, it remains a critical anchor for silicon correlation. Research indicates that up to 35% of silicon failures in advanced nodes can only be detected through GLS, particularly those related to timing, power-aware verification, and complex X-propagation.

Verification Aspect	RTL Simulation	Gate-Level Simulation (GLS)
Timing Accuracy	Zero-Delay / Ideal	SDF-Based (Real Timing)
X-Propagation	Limited / Pessimistic	High (Physical Accuracy)
Power Management	Behavioral	Accurate (Power-Gating/Clock-Gating)
Silicon Correlation	Low to Medium	High

The Shift-Left framework uses RTL for rapid iterations and early bug discovery, but it employs a targeted GLS strategy for final sign-off. This ensures that the physical effects introduced by synthesis and layout such as metal resistance and voltage drop are accounted for before tape-out.

6. Post-Silicon Validation and Diagnostics

Once the silicon is manufactured, the DFT infrastructure becomes the primary tool for validation and failure analysis. Silicon correlation is proven when the failing signatures on the tester can be accurately traced back to the pre-silicon models.

Scan Chain Diagnosis and Root Cause Analysis (RCA)

When a chip fails a manufacturing test, scan chain diagnosis is used to pinpoint the defect. By analyzing the shift-in and shift-out patterns, diagnostic tools can isolate the failing flop or net. Silicon correlation is confirmed if the physical defect identified via failure analysis techniques like scanning electron microscopy (SEM) matches the logical location predicted by the pre-silicon diagnostic simulation.

Statistical analysis, including Monte Carlo simulations and Shmoo plotting (varying voltage, frequency, and temperature), is used to identify the boundaries of failure. This data is fed back into the pre-silicon models to improve the accuracy of future designs, creating a continuous improvement loop.

Silicon Lifecycle Management (SLM)

Modern Shift-Left frameworks are increasingly integrating with Silicon Lifecycle Management (SLM) solutions. SLM extends the role of DFT throughout the entire life of the product. On-chip monitors (PVT sensors, aging monitors) provide real-time data on the chip's health, which can be correlated with the initial manufacturing test data to predict potential field failures.

The integration of SLM ensures that the "Scan Quality" shifted left during the design phase is maintained throughout the product's deployment. In sectors like automotive electronics, where functional safety and long-term reliability are paramount, this lifecycle-long correlation is a critical requirement.

Future Outlook: AI/ML and 3D Integration

The future of Shift-Left DFT lies in the adoption of AI and ML to further automate the verification and correlation processes. AI-enabled ATPG tools are beginning to learn from historical silicon data to optimize pattern generation, while ML-based TPI prediction can identify testability bottlenecks even earlier in the architectural phase.

Furthermore, as the industry moves toward 3D-integrated circuits and chiplet-based architectures, the hierarchical DFT framework must evolve to handle vertical test access and inter-die connectivity. These multi-die systems present unique challenges for silicon correlation, requiring standardized interfaces (like IEEE 1838) and more sophisticated cross-layer verification strategies.

7. Conclusion

The shift toward a hierarchical RTL-based DFT verification framework is an essential response to the escalating complexity of sub-5nm semiconductor design. By Shifting-Left, designers can proactively address testability challenges, optimize PPA concurrently with synthesis, and drastically reduce the time-to-market for complex SoCs. This research has demonstrated that a successful framework relies on a hierarchical partitioning strategy, robust core-wrapping standards, and the early use of RTL-level DRC and Test Point Insertion tools.

Furthermore, the study emphasizes that the value of any pre-silicon framework is contingent upon its silicon correlation. By integrating functional fault grading and maintaining a targeted loop with gate-level simulation and post-silicon diagnostics, designers can ensure that their test coverage metrics are not just theoretical abstractions but proven indicators of product quality. As the industry moves into the era of AI-driven design and heterogeneous 3D integration, these Shift-Left principles will remain the cornerstone of achieving zero-defect silicon and long-term product reliability.

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